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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/605,323	09/23/2003	CHIH-HUNG CHIANG	10680-US-PA	2322

31561 7590 12/22/2004

JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE
7 FLOOR-1, NO. 100
ROOSEVELT ROAD, SECTION 2
TAIPEI, 100
TAIWAN

EXAMINER
NGUYEN, THANH NHAN P

ART UNIT	PAPER NUMBER
2871	

DATE MAILED: 12/22/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/605,323	CHIANG ET AL.	
	Examiner	Art Unit	
	(Nancy) Thanh-Nhan P Nguyen	2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 September 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

The drawings are objected to because of the following informalities:

FIGS. 2-4 are presently stated as "PRIOR ART". It appears that they should have meant for the present invention and have been examined accordingly.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) The invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 5-8 are rejected under 35 U.S.C. 102(b) as being anticipated by Sakamoto et al U.S. Patent Application Publication No. 2003/0030768.

Referring to claim 1, Sakamoto et al discloses a pixel structure comprising a gate line (1), located on a substrate (8); a common line (4), located on substrate for a bottom electrode of a pixel storage capacitor; a gate insulating layer (9), located on substrate, and gate insulating layer covering gate line and common line; a data line (2), located on gate insulating layer; a switching device (TFT 3), located on substrate, said switching device electrically connecting to gate line and data line; a conducting layer (drain electrode extended), located on gate insulating layer, said conducting layer including a coupling portion and a connecting portion, said coupling portion being above common line for a top electrode of pixel storage capacitor, said connecting portion connecting coupling portion and switching device; a passivation layer (10), covering data line, switching device, and conducting layer; a contact window (7), disposed in passivation layer and above connecting portion ; and a pixel electrode, located on passivation, said pixel electrode electrically connecting to switching device and coupling portion of conducting layer through contact window, [see figs. 1 and 2].

Referring to claim 5, Sakamoto et al discloses a pixel structure, further comprising a planarization layer (11) (made of an organic substance, [see paragraph 0010]) between passivation and pixel electrode, [see fig. 2].

Referring to claim 6, Sakamoto et al discloses a switching device is a thin film transistor (3), said thin film transistor comprising a gate electrode (1a) connected to said gate line; a source electrode and a drain electrode on channel layer, said source electrode being electrically connected to data line, said drain electrode being electrically connected to connecting portion of conducting layer, [see figs. 1 and 2].

Sakamoto et al does not show the channel layer on the gate insulating layer above gate electrode, however, the channel layer is inherent with thin film transistor. The thin film transistors that are fabricated by consecutive deposition of the gate, drain and source electrode, and the gate insulator have to have the semiconductor channel material in the region between the source electrode and drain electrode and overlapping the gate electrode. Otherwise, the device would not function as a transistor.

Referring to claim 7, Sakamoto et al discloses the gate line is parallel to common line in the pixel structure, [see fig. 1].

Claim 8 is met the discussion regarding claims 1 and 6 rejection above.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2-4, 9-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakamoto et al in view of Matsueda U.S. Patent No. 5,173,792.

Referring to claims 2-3, Sakamoto et al lacks disclosure of the connecting portion of conducting layer is a multi-channel structure, said connecting portion comprising a first portion coupled to coupling portion; a second portion connected to switching device; and a third portion between first portion and second portion, said third portion including a plurality of channels; wherein contact window is disposed in passivation layer and above one of plurality of channels of third portion.

Matsueda discloses the connecting portion of conducting layer is a multi-channel structure, said connecting portion comprising a first portion (170A, 170B, 170C) coupled to coupling portion; a second portion (at contact window (165) region) connected to switching device; and a third portion between first portion and second portion, said third portion including a plurality of channels (151, 152, 153); wherein contact window (165) is disposed in passivation layer (148) and above one of plurality of channels (170") of third portion, [see figs. 11 and 12], for the benefit of correcting the defective display element circuits in the fabricated display thereby increasing their manufacturing yield,

[see col. 1, lines 11-14; col. 15, lines 62-68]. Therefore, at the time the invention was made, it would have been obvious to a person of ordinary skill in the art to use a connecting portion of conducting layer having multi-channel structure for the benefit of correcting the defective display element circuits in the fabricated display thereby increasing their manufacturing yield.

Referring to claim 4, it was well known to use a blocking layer below connecting portion in the pixel structure to prevent the light leakage for having higher contrast in liquid crystal display device. Therefore, at the time the invention was made, it would have been obvious to a person of ordinary skill in the art to use a blocking layer below connecting portion in the pixel structure for the benefit of preventing the light leakage to have higher contrast in liquid crystal display device.

Referring to claim 12, it was well known to have blocking layer formed in a common area during forming gate electrode, gate line, and common line for the benefit of reducing steps in manufacturing to have higher production. Therefore, at the time the invention was made, it would have been obvious to a person of ordinary skill in the art to form blocking layer in common area during forming gate electrode, gate line, and common line for the benefit of having higher production.

Claim 9 is met the discussion regarding claims 1, 2 and 6 rejection above.

Claim 10 is met the discussion regarding claims 1, 3, and 6 rejection above.

Claims 11 is met the discussion regarding claims 1, 4, and 6 rejection above.

Claim 13 is met the discussion regarding claims 1, 5, and 6 rejection above.

Claim 14 is met the discussion regarding claims 1, 6, and 7 rejection above.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Sakamoto et al U.S. Patent Application Publication No. 2003/0030768 discloses the pixel structure comprising a conducting layer having a portion above common line for a top electrode of pixel storage capacitor.

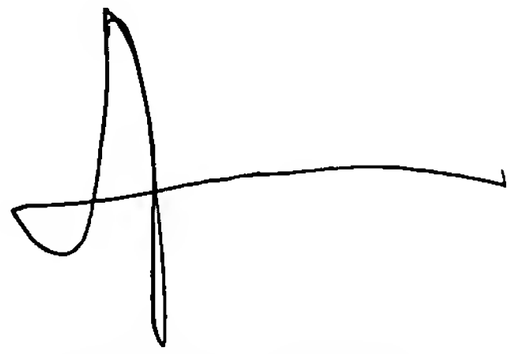
Matsueda U.S. Patent No. 5,173,792 discloses the connecting portion of conducting layer is a multi-channel structure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to (Nancy) Thanh-Nhan P Nguyen whose telephone number is 571-272-1673. The examiner can normally be reached on M-F/9-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Kim can be reached on 571-272-2293. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

(Nancy) Thanh-Nhan P Nguyen
Examiner
Art Unit 2871



KENNETH PARKER
PRIMARY EXAMINER